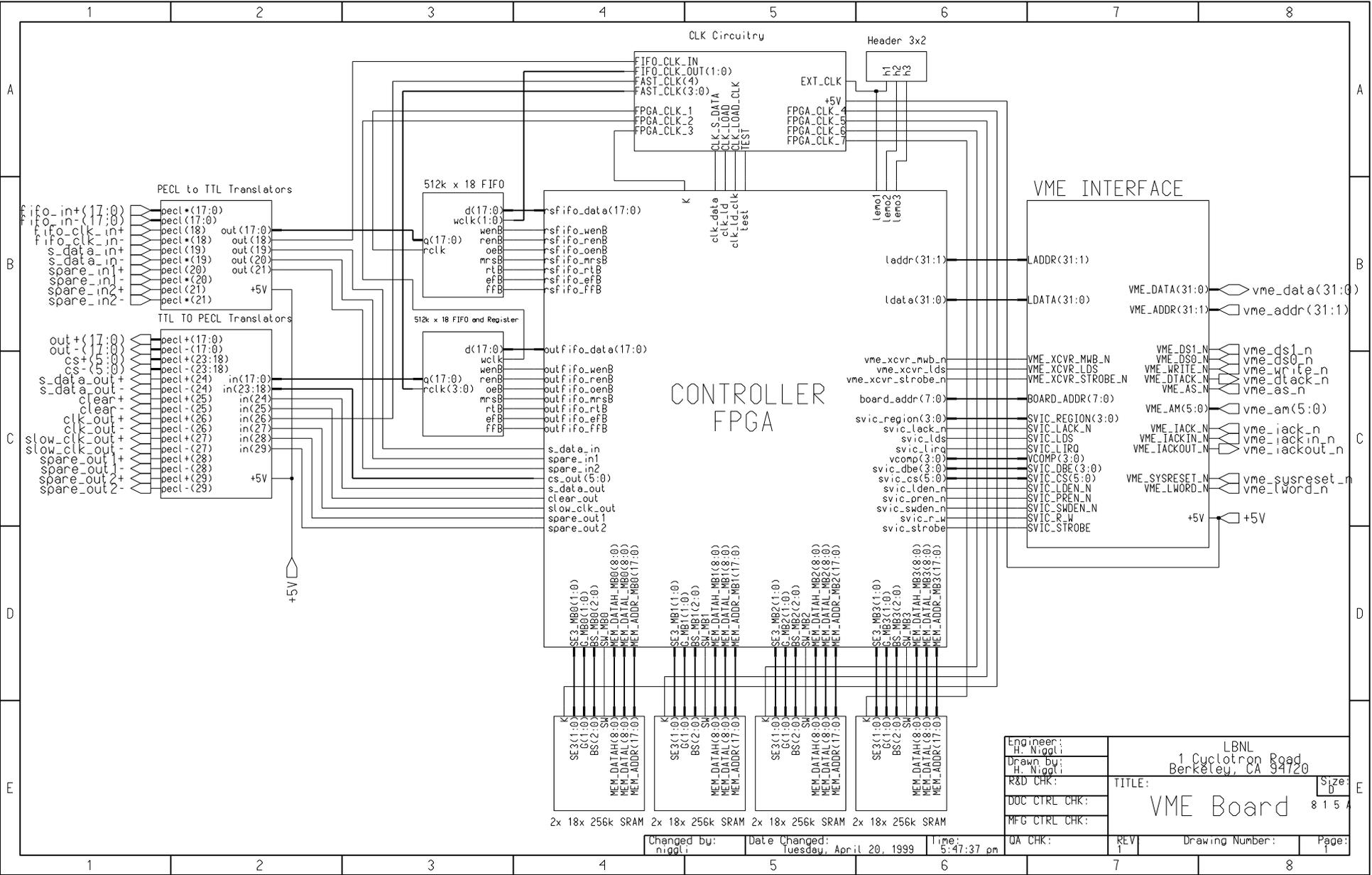
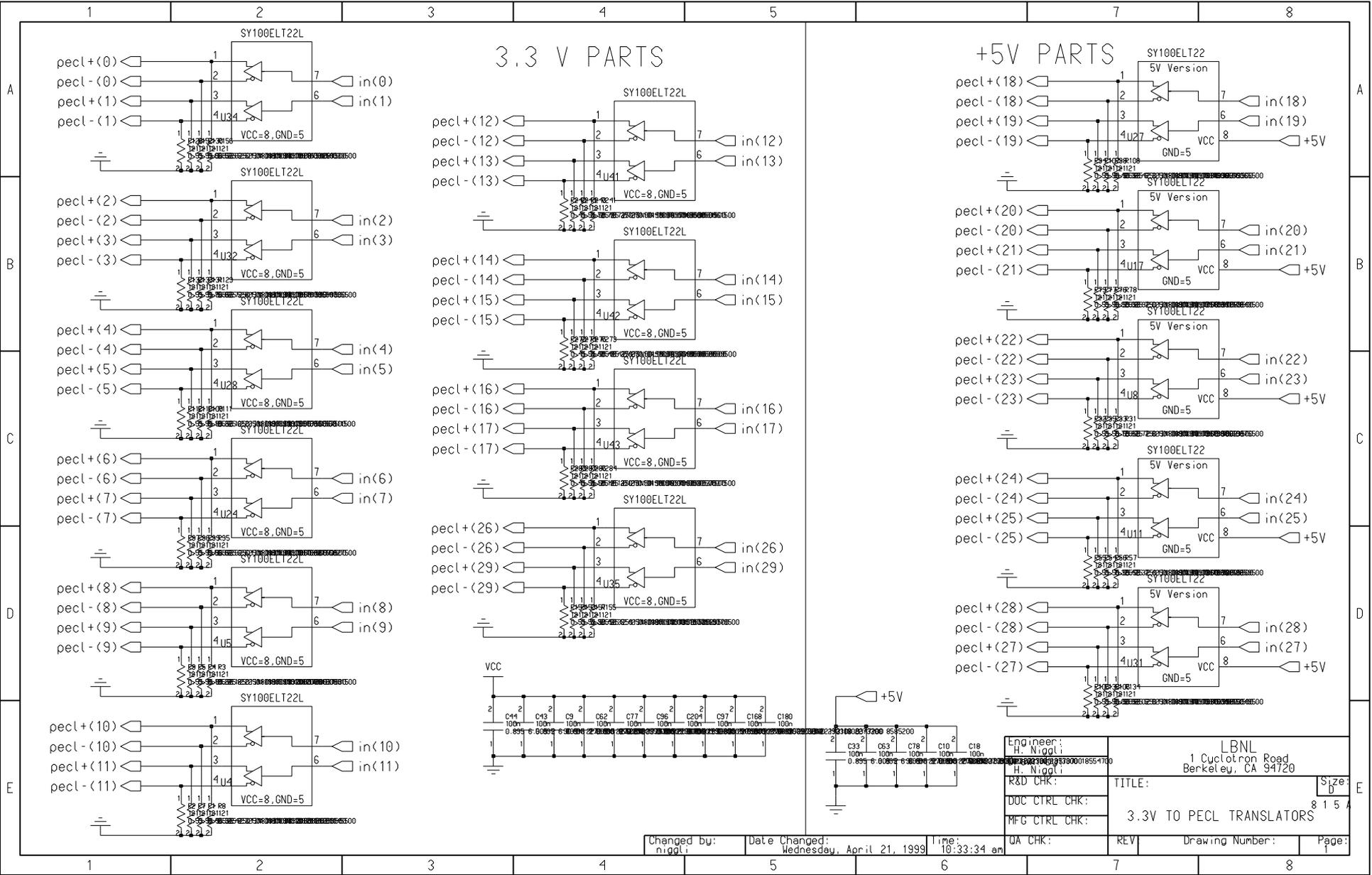


Engineer:	H. Niggl	1 LBNL
Drawn by:	H. Niggl	1 Cuclotron Road
RDW CHK:		Berkeley, CA 94720
DOC CTRL CHK:	VME Board	Size E
FIG ENGR CHK:	Top Level/ Connectors	1 of 1



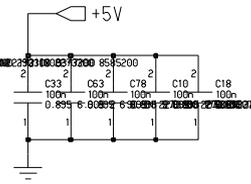
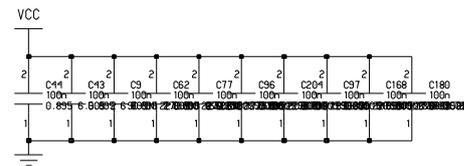
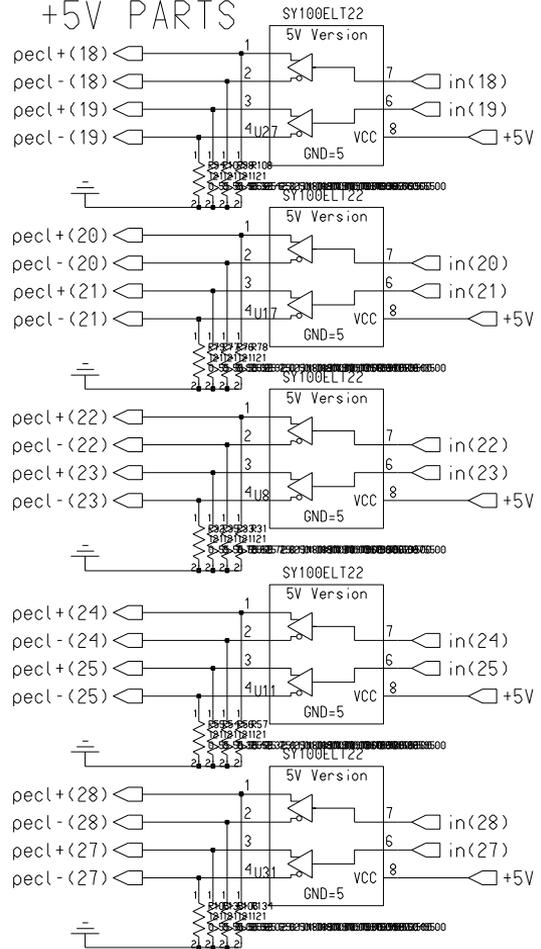
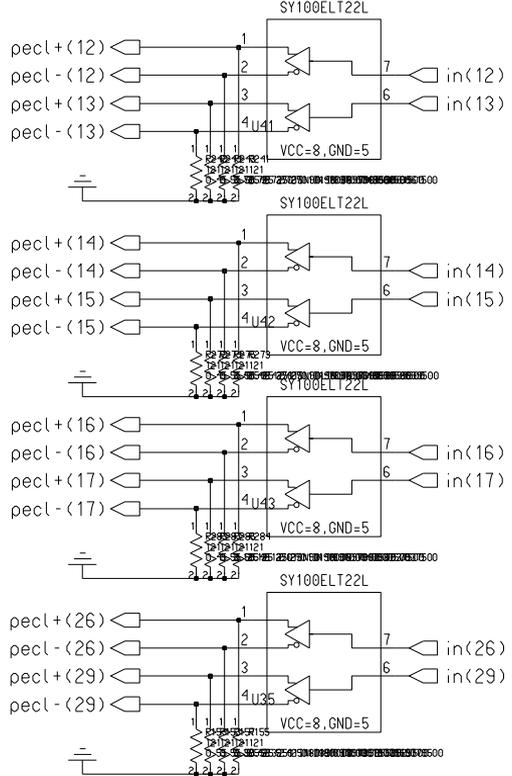
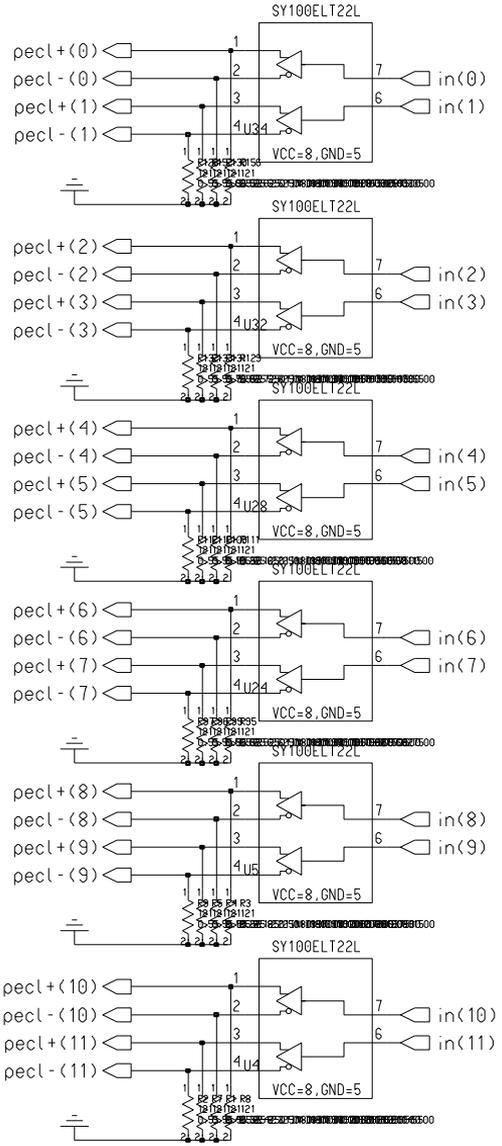
Engineer: H. Niggli	LBNL 1 Cyclotron Road Berkeley, CA 94720		Size: 8 1 5 A
Drawn by: H. Niggli	TITLE:	VME Board	
R&D CHK:	DOC CTRL CHK:	MFG CTRL CHK:	QA CHK:
REV: 1	Drawing Number:	Page: 1	

Changed by: niggli Date Changed: Tuesday, April 20, 1999 Time: 5:47:37 pm



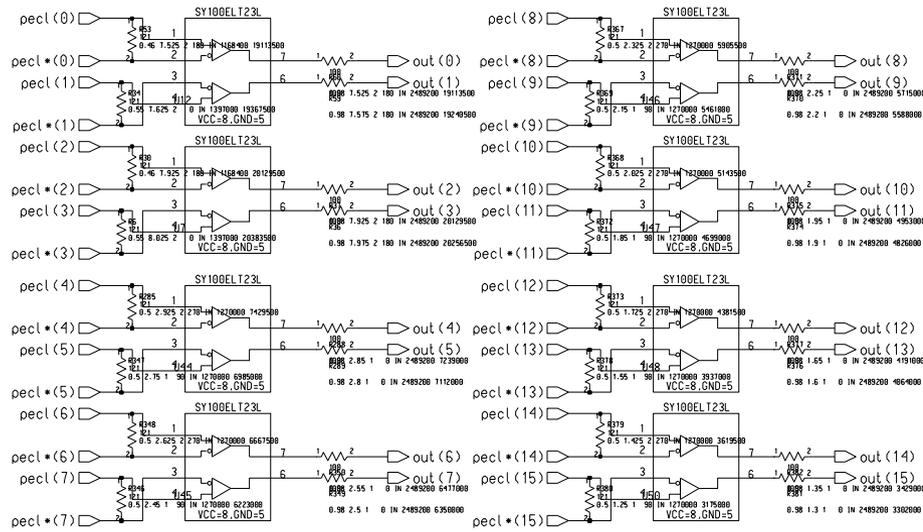
3.3 V PARTS

+5V PARTS

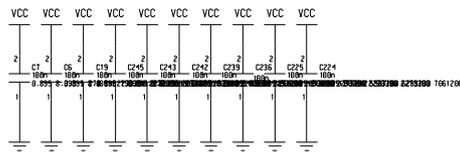
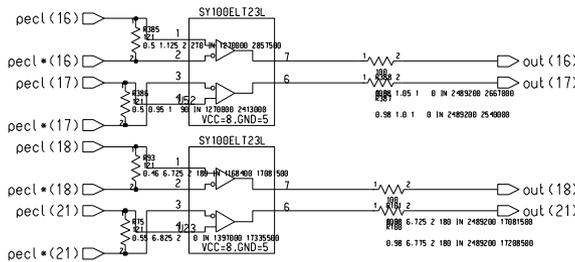


Engineer: H. Nigol	TITLE: 3.3V TO PECL TRANSLATORS	Size: 15 A
R&D CHK: H. Nigol	TITLE: 3.3V TO PECL TRANSLATORS	
DOC CTRL CHK:		
MFG CTRL CHK:		
QA CHK:	REV:	Page: 1
Drawing Number:		

3.3 V PARTS

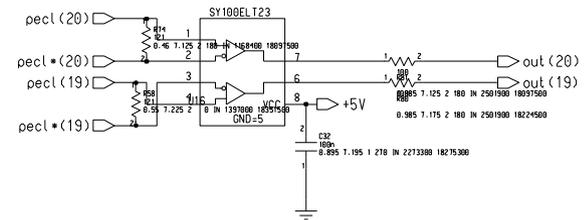


all outputs 100 Ohm traces



PLACE 1 CAP AT EACH VCC PIN

5 V PARTS



Engineer: H. Niggli	LBNL 1 Cyclotron Road Berkeley, CA 94720		Size: c
Drawn by: H. Niggli	TITLE:	LVPECL Receivers	
R&D CHK:			4 1 4 A
DOC CTRL CHK:			
MFG ENGR CHK:			
Changed by: niggli	Date Changed: Wednesdu, April 21, 1999	Time Changed: 10:16:18 am	Page: 1

WCLK: 100 Ohm

ntB
mrsB

rc1n
rc0n
rc1b
rc0b
wclka
wclkb
wenb

VCC

VCC
C152 C153 C151

VCC
C128 C119 C99

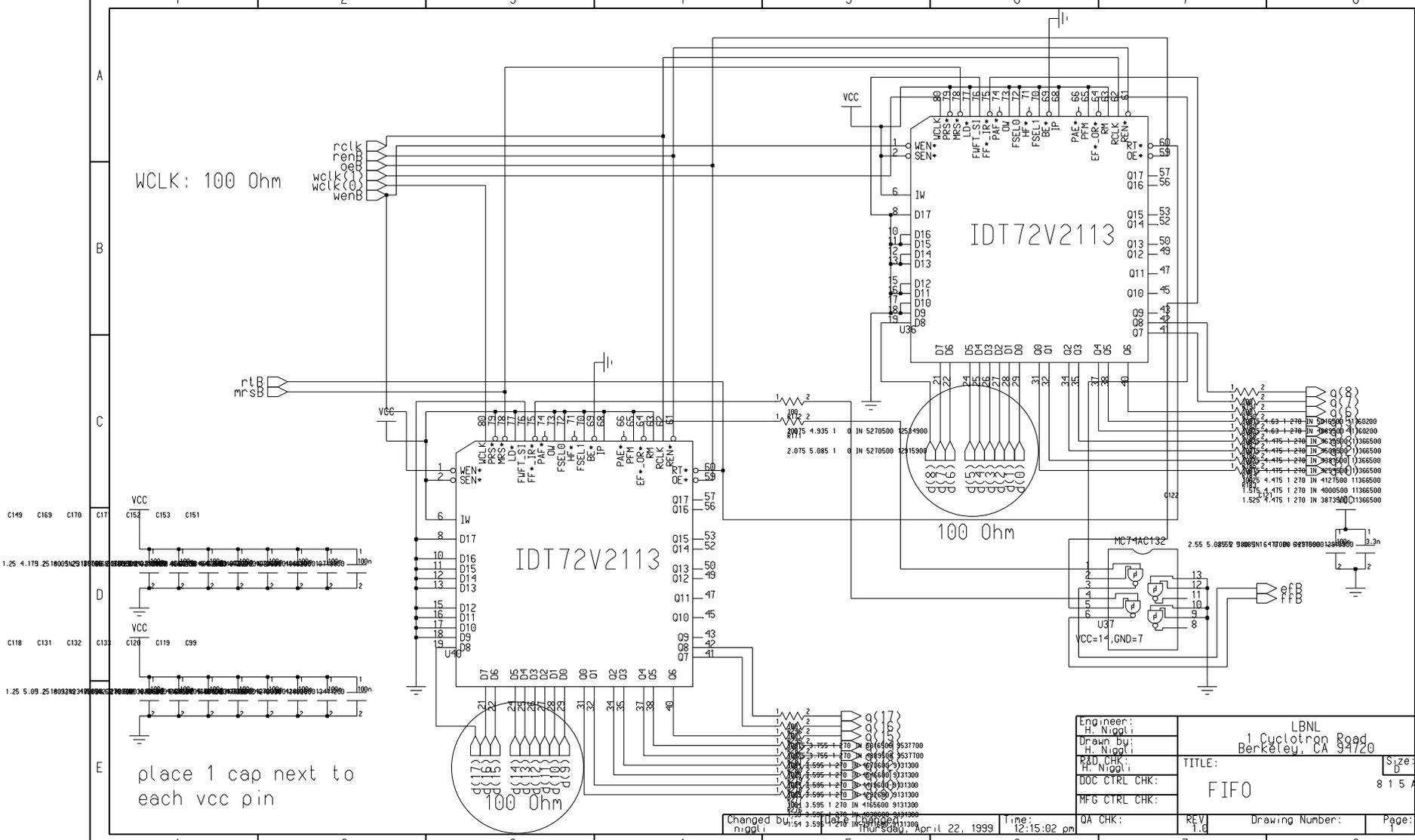
place 1 cap next to each vcc pin

IDT72V2113

IDT72V2113

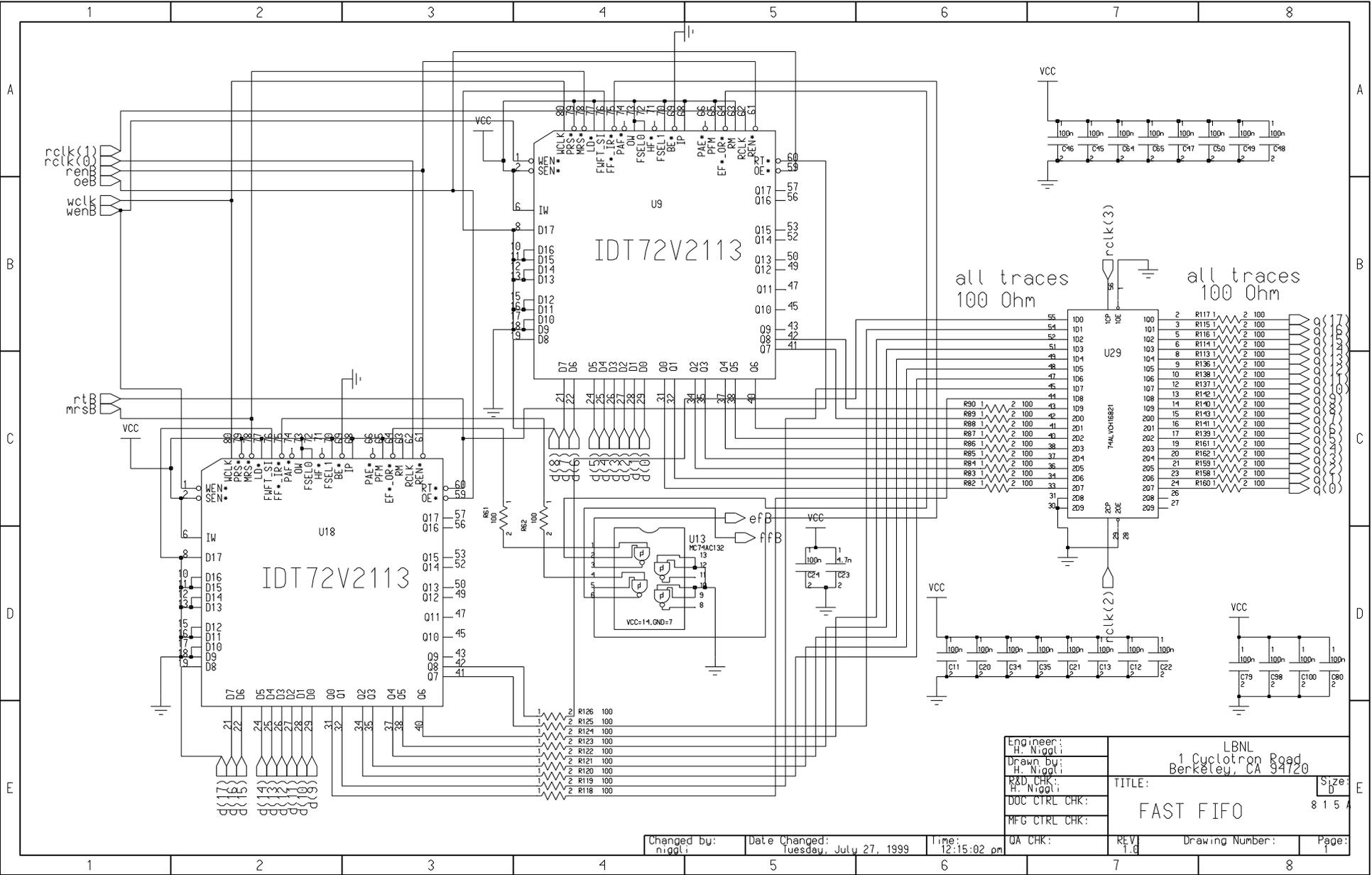
100 Ohm

100 Ohm

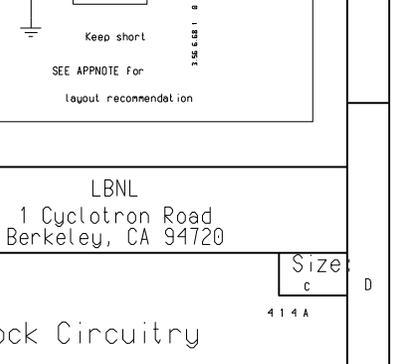
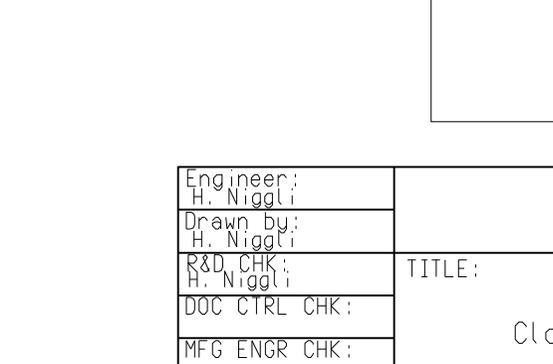
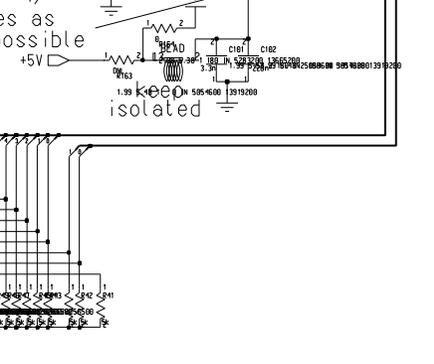
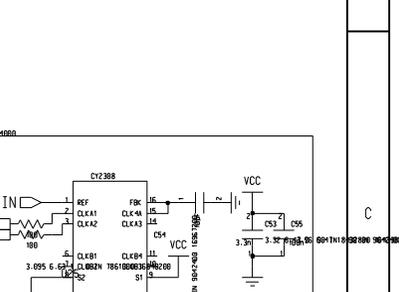
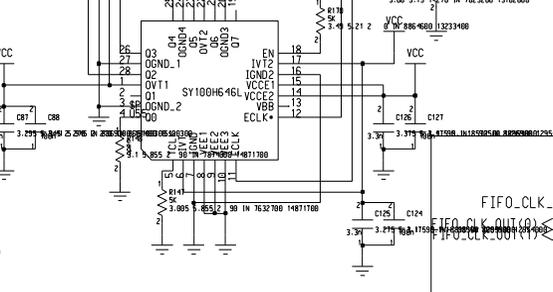
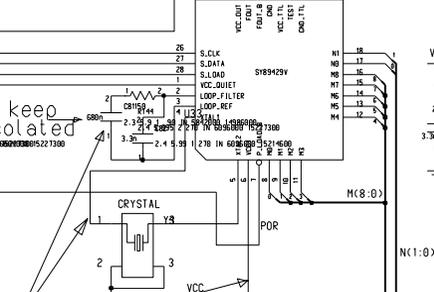
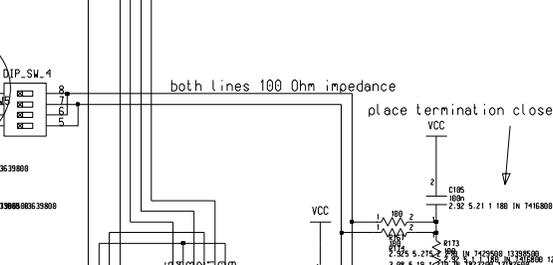
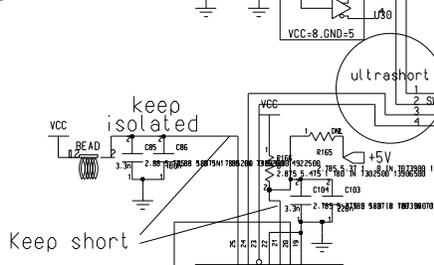
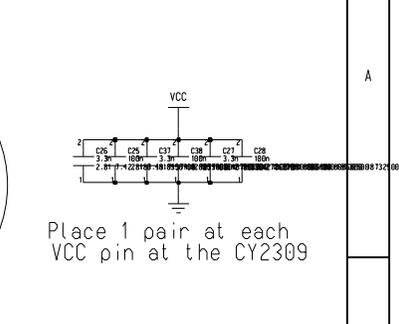
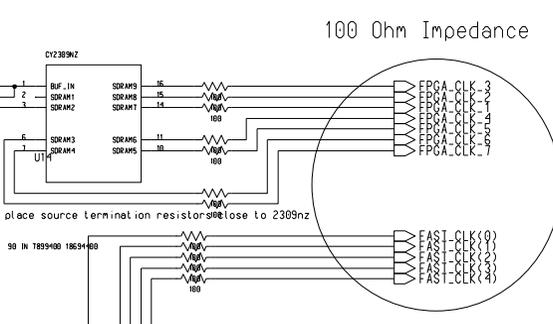
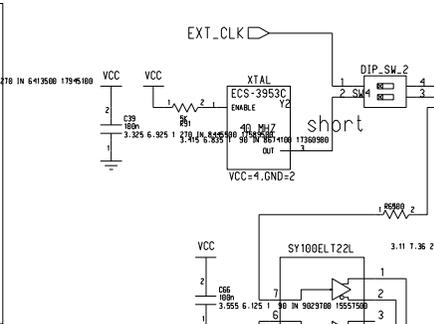
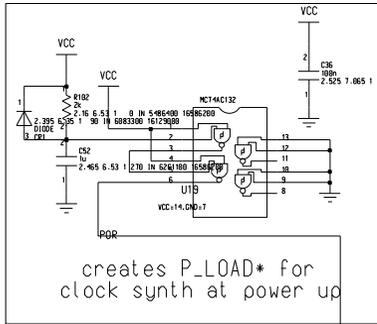


Engineer: H. Niggl	1 Cyclotron Road Berkeley, CA 94720		Size 8 1 5 A
Drawn by: H. Niggl	TITLE: FIFO		
RAD CHK:			
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV: 1.0	Drawing Number:	Page: 1

Changed by: niggli
Date: Thu, 22 Apr 1999 12:15:02 pm



Engineer:	LBNL	
Drawn by:	1 Cyclotron Road	
R&D CHK:	Berkeley, CA 94720	
DOC CTRL CHK:	TITLE:	FAST FIFO
MFG CTRL CHK:	REV:	1.0
QA CHK:	Drawing Number:	8154



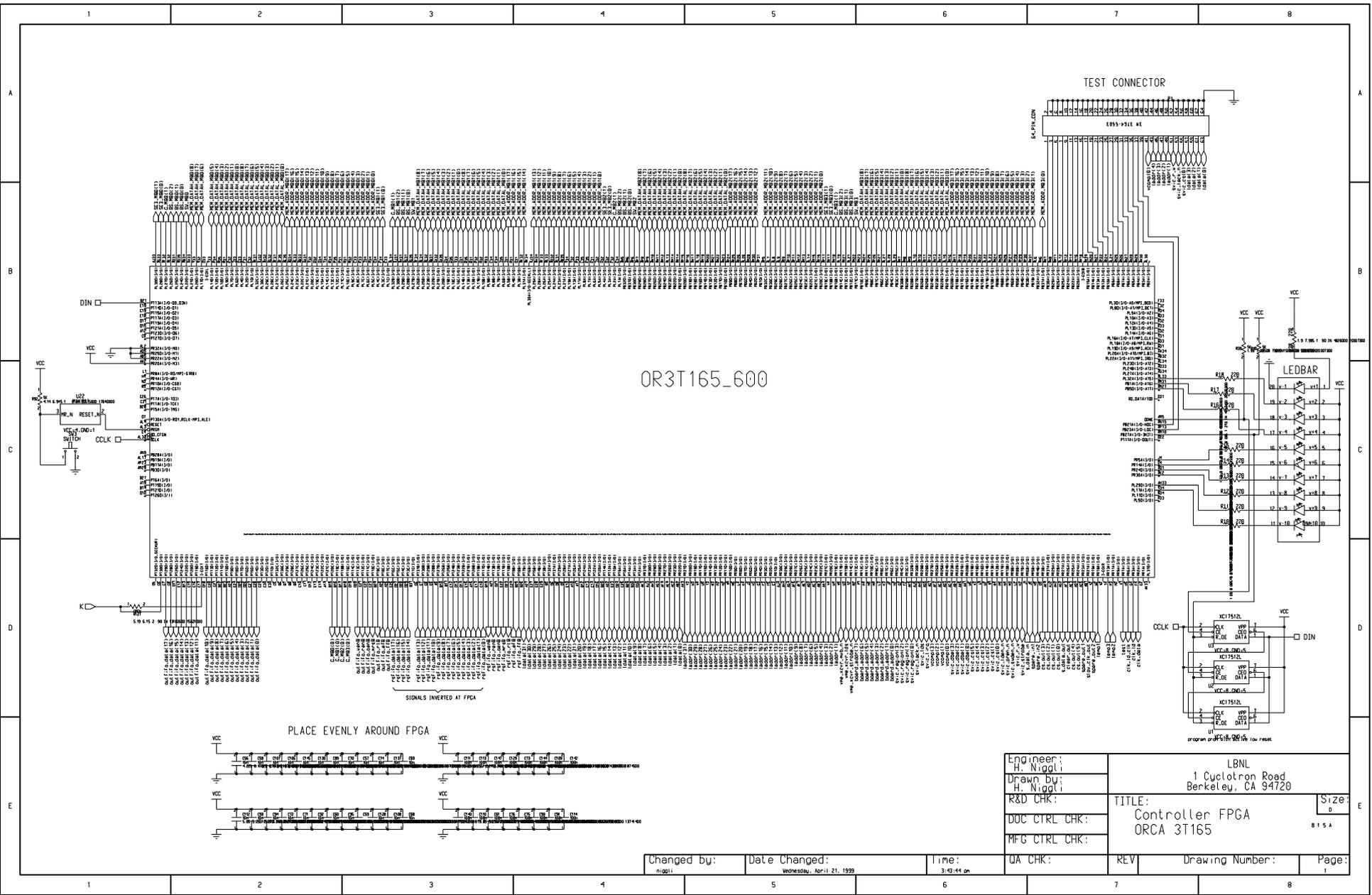
Engineer: H. Niggli
 Drawn by: H. Niggli
 R&D CHK: H. Niggli
 DOC CTRL CHK:
 MFG ENGR CHK:

LBNL
 1 Cyclotron Road
 Berkeley, CA 94720

TITLE: Clock Circuitry

Size: 114A

Changed by: niggli	Date Changed: Wednesday, April 21, 1999	Time Changed: 2:36:54 am	QA CHK:	REV: 1.0	Drawing Number:	Page: 1
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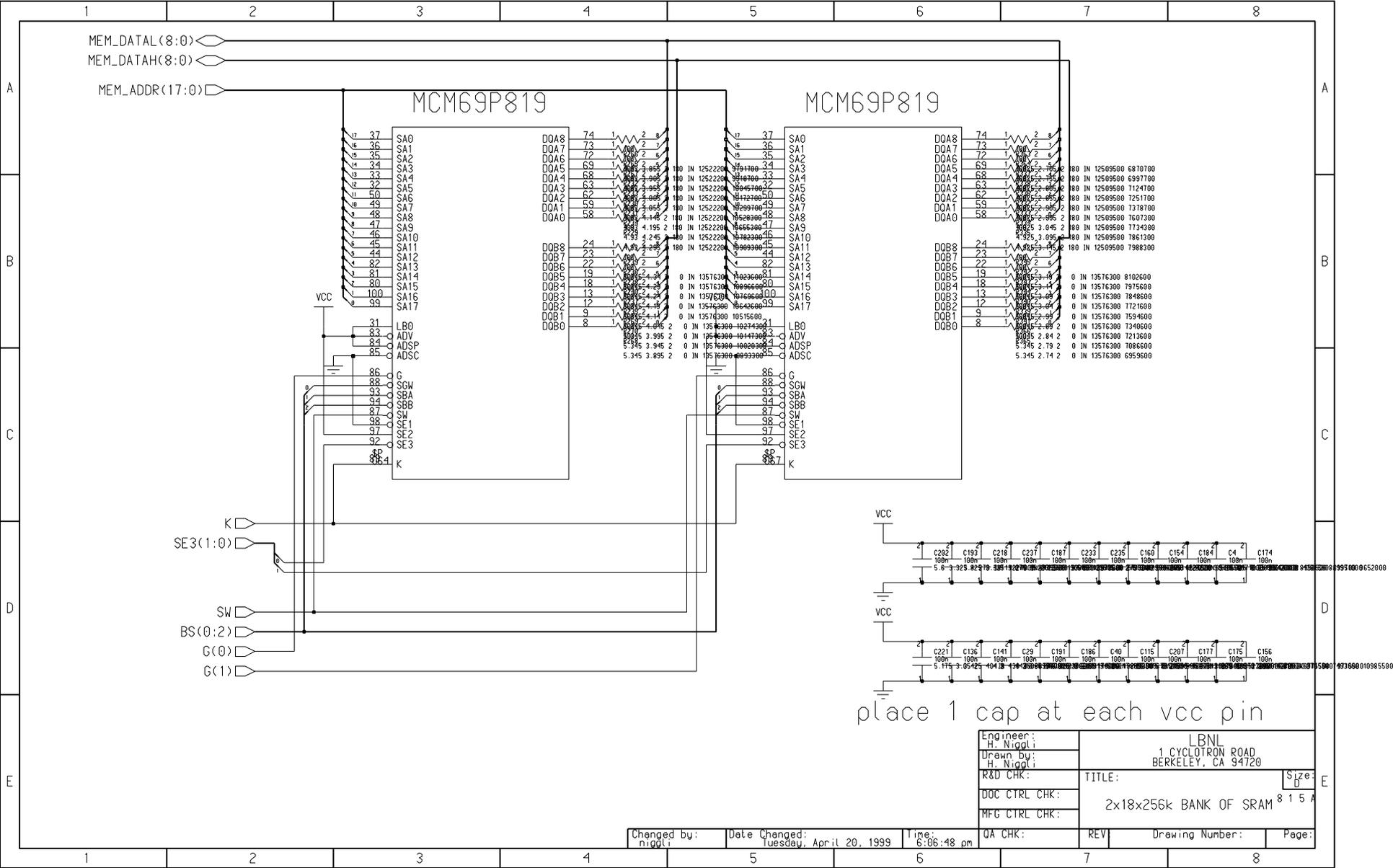


OR3T165_600

SIGNALS INVERTED AT FPGA

PLACE EVENLY AROUND FPGA

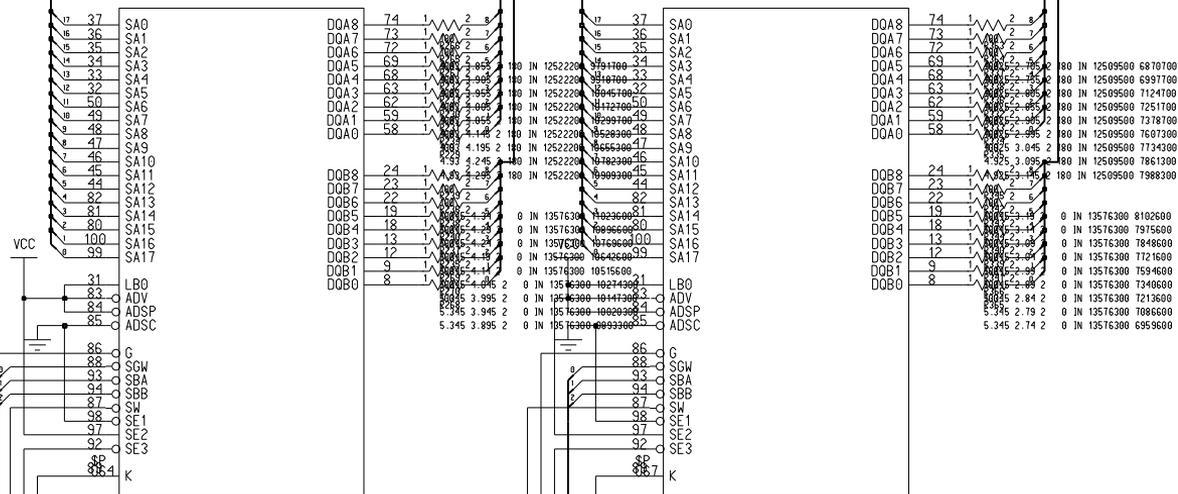
Engineer:	H. Niigoi	LBNL 1 Cyclotron Road Berkeley, CA 94720	Size: D
Drawn by:	H. Niigoi		
R&D CHK:		TITLE:	ORCA 3T165
MFG CTRL CHK:		REV:	815A
QA CHK:		Drawing Number:	
Changed by:	nigoi	Date Changed:	Wednesday, April 21, 1999
		Time:	3:43:44 pm
			Page:



MEM_DATA(8:0)
MEM_DATAH(8:0)
MEM_ADDR(17:0)

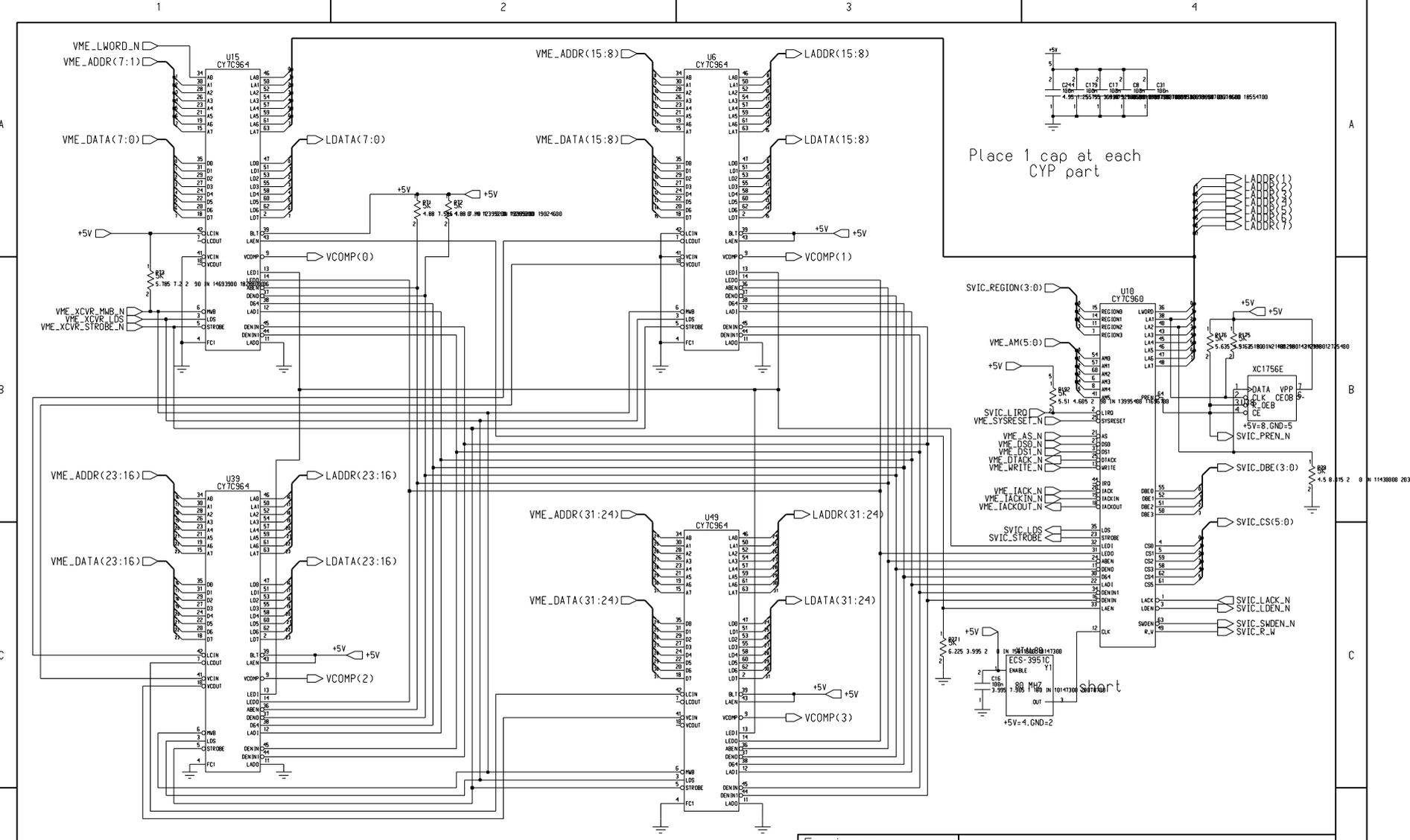
MCM69P819

MCM69P819



place 1 cap at each vcc pin

Engineer: H. Niggl	LBNL 1 CYCLOTRON ROAD BERKELEY, CA 94720
Drawn by: H. Niggl	TITLE: 2x18x256k BANK OF SRAM
R&D CHK:	Size: 8 1 5 4
DOC CTRL CHK:	
MFG CTRL CHK:	



Place 1 cap at each CYP part

ALL IC'S ON THIS SCHEMATIC HAVE +5V SUPPLY VOLTAGE

Engineer: K. Dao	LBL 1 Cyclotron Road Berkeley, CA 94720		Size: c
Changed by: H. Nigali	TITLE: VME Interface (based on Pixel PLL VME Int.)		414 A
R&D CHK:	DOC CTRL CHK:	REV:	Page: 1
MFG ENGR CHK:	QA CHK:	Drawing Number:	

1

2

3

4

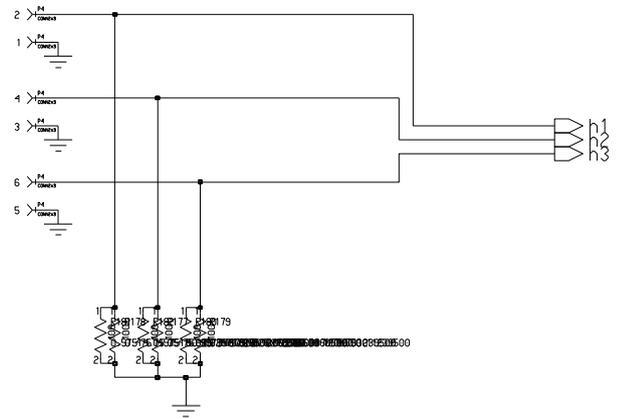
A

A

EXTERNAL INPUT

EXTERNAL INPUT

EXTERNAL OUTPUT



B

B

C

C

Engineer: H. Niggli	LBNL 1 Cyclotron Road Berkeley, CA 94720		
Drawn by: H. Niggli			
R&D CHK:	TITLE:	Size: B	
DOC CTRL CHK: H. Niggli	Lemo Connectors		4 1 4 A
MFG ENGR CHK:	D		
Changed by: niggli	Date Changed: Tuesday, April 20, 1999	Time Changed: 5:45:49 pm	
QA CHK:	REV 1.0	Drawing Number:	Page: 1

D

D

1

2

3

4